

A Low Budget Vector Network Analyzer for AF to UHF

The author's PC turned his "simple gadget" into a sophisticated piece of test equipment.

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Introduction

After years of professional work with commercial vector network analyzers (VNWAs), I did not want to miss this handy kind of test equipment in my shack at home any longer. Looking through the surplus market, I found that the price for a commercial VNWA is still well out of reach for the average hobbyist. At that time, a *QEX* article on a homebrew VNWA caught my attention.¹ Some Internet research revealed another similar project by N2PK.² Both projects have in common the use of direct digital synthesizer (DDS) circuits to generate an RF test signal and an LO signal for down-converting the tested component's response signals to zero IF. The dc IF signals are then digitized by appropriate analog-to-digital converters. The digital numbers are fed into a standard personal computer (PC) for further processing and imaging.

I found that concept very attractive; but coming from the analog side of electronics design, I thought about ways to simplify the analog section and cut down as much as possible on the digital components, consisting of A/D converters and a microcontroller at the least. Clearly, there was no reasonable substitute for the DDS oscillators. But I found that all other digital and mixed-signal tasks could be performed by the standard PC. I

¹Notes appear on page 53.

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intended to tie the DDS oscillators directly to the parallel PC printer interface and to make use of the standard PC stereo sound card for analog signal acquisition. Thus a very simple concept took shape in my mind. All that was needed to build a VNWA were two DDS oscillator chips, an SWR bridge and three mixers (through, reflect and reference). I assembled a first prototype in a cardboard box within a few days. That's where the adventure started.

Had I known beforehand how many software problems I had to solve, I might never have started the project. However, after about a year of heavy learning and coding, the PC has turned my simple little gadget into an accurate piece of RF test equipment.

Why Vector Network Analysis?

Did you ever want to match a crystal filter systematically to obtain a perfectly flat pass-band? Or did you ever want to know the ca-

pacitance value of that special SMD capacitor or the Q value of your homemade inductor? A vector network analyzer is the perfect choice to solve all these problems. When you analyze an RF component like a filter, or an antenna, you are typically interested in the return loss and/or in the insertion attenuation of the component in a specific frequency range. This information can be obtained with a scalar network analyzer, which basically consists of a signal source, an SWR bridge and an RF detector. The return loss is defined as the power reflected from the device input divided by the input power incident into the device. The insertion attenuation equals the output power of the device divided by the incident input power.

Vector network analyzers do not only measure these signal power ratios but also the phase increments from input signal to reflected and/or transmitted signal. On first sight, these phase values seem uninteresting;

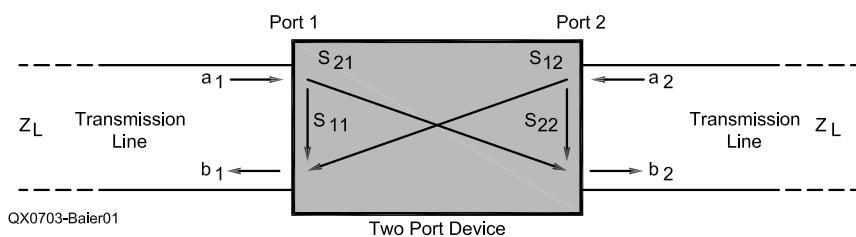


Figure 1 — Connection between S-parameters and incident and evanescent waves at an electrical two port device.

but a closer look reveals that it is these phases that enable us to calculate impedance values and use the measurement results in system simulations with software tools like APLAC or ADS,^{3,4} to calculate the behavior of the test object at modified termination impedance levels. The theory behind this is the theory of scattering parameters or S parameters. The set of S parameters, also called S matrix, completely describes the linear properties of an RF device. A VNWA is designed to measure these S-parameters.

Two-Port S Parameters

To completely characterize the linear properties of a two port RF device (like an IF filter) at a given frequency, four S-parameters are required, which are combined to form the two-port S-matrix:

$$\begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix}$$

S-parameters are complex numbers; that is, they consist of a magnitude (=attenuation) and a phase value. As shown in Figure 1, they relate incident wave amplitudes a_i to reflected and transmitted wave amplitudes b_i :

$$\begin{aligned} b_1 &= S_{11} \cdot a_1 + S_{12} \cdot a_2 \\ b_2 &= S_{21} \cdot a_1 + S_{22} \cdot a_2 \end{aligned} \quad [\text{Eq 1}]$$

While indices=1 denote waves on the device input, indices=2 denote waves on the device output.

At this point, it becomes clear how to measure S parameters. To measure S_{21} , make sure that there is only one wave a_1 incident from the left side. Measure it and measure also the wave b_2 transmitted through the de-

vice under test (DUT). Since $a_2 = 0$ (no wave incident to the output of the DUT from the right hand side) S_{21} can simply be obtained: $S_{21} = b_2/a_1$.

S_{11} can be obtained in a similar manner by additionally measuring the reflected wave from the DUT input b_1 : $S_{11} = b_1/a_1$.

S_{12} and S_{22} can be measured in the very same way by exchanging DUT input and output. Commercial two-port VNWAs achieve this DUT reversal with built-in switches. The simpler homebrew method is to interchange the connectors during the S-parameter acquisition.

Now, the test condition $a_2 = 0$ needs a little additional consideration. It means that there is no RF power propagating into the DUT output from the right hand side. Of course, we are not about to connect an oscillator to the DUT output while measuring S_{21} . But there is another source for such a signal, namely the wave reflected from the signal detector at the DUT output. Reflection always takes place when the detector input impedance is unequal to the transmission line impedance Z_L (usually 50 Ω) it connects to. Similarly, care has to be taken that the signal source impedance of the VNWA on the DUT input side is properly matched to the transmission line impedance. Otherwise the wave b_1 reflected from the DUT back to the VNWA will be re-reflected at the oscillator interface back into the DUT and introduce an error on a_1 .

VNWA Design

Figure 2 shows the basic design of my VNWA. It consists of two digitally tunable DDS oscillators. The RF oscillator generates a wave a_1 which is running through an

SWR bridge to the DUT. The bridge is used to measure the incident wave a_1 (reference signal) and the reflected wave b_1 (reflect signal). The wave b_2 transmitted through the DUT is also measured (through signal). All these test signals are mixed down with a DDS local oscillator to an IF signal in the audio frequency range that can be processed by a PC sound card. This is one of the special features of my design to simplify the VNWA. Since a standard PC sound device has only two simultaneously sampled signal inputs, namely stereo left and right, some kind of switch is required to multiplex the three test signals to the two audio channels. Care has to be taken to achieve a sufficiently high switch isolation of about 100 dB. Alternatively, one could add a second sound card to the PC. The current software version does not support two sound cards, though. Since most sound cards utilize 16 bit AD-converters, a dynamic range of $20 \cdot \log(2^{16})$ dB \approx 96 dB is to be expected and indeed, also realized. Experiments with a 24-bit sound card⁵ yielded no significant improvement of the dynamic range (theoretically 144 dB) though, since the least significant data byte is dominated by noise and on top, a systematic phase error between left and right channel was observed.⁶

In the Labyrinth of a Microsoft Windows PC

The PC's tasks are basically quite simple now:

1. Set DDS oscillators to new test frequency.
2. Wait until DUT reaches steady state (especially important for DUTs with high Q-values).

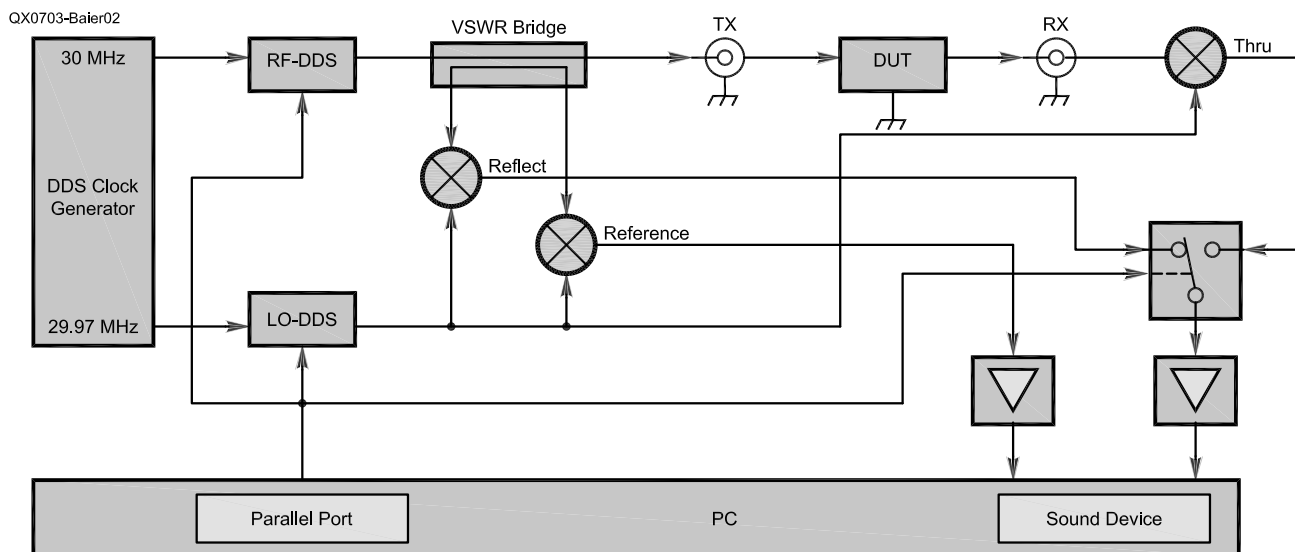


Figure 2 — Basic construction of the described vector network analyzer.

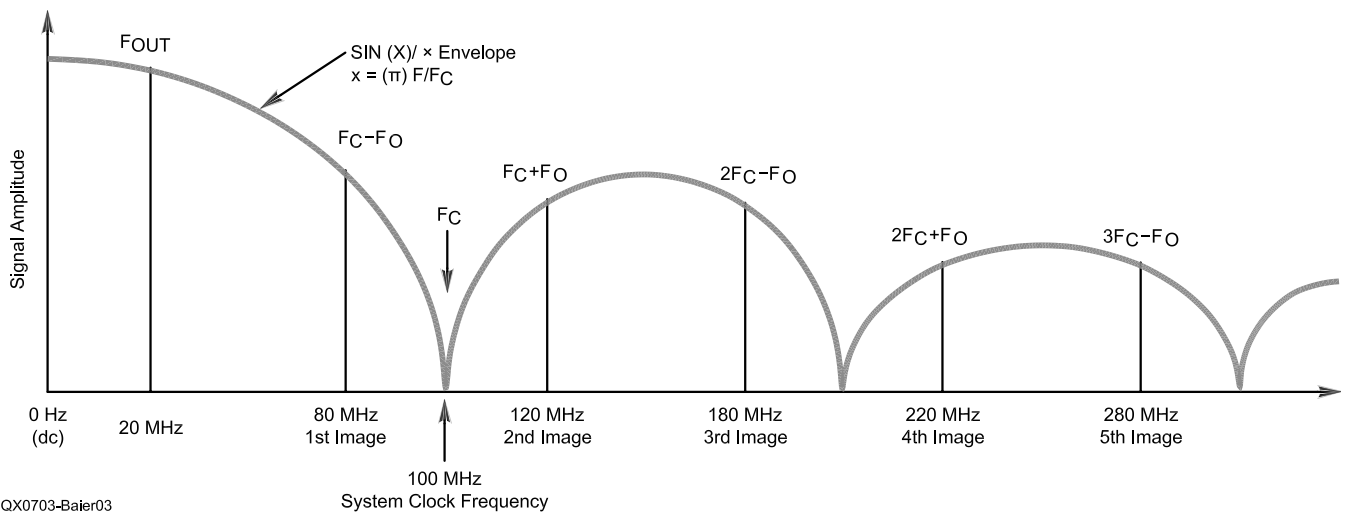


Figure 3 — Unfiltered output spectrum of a DDS oscillator (from Note 7).

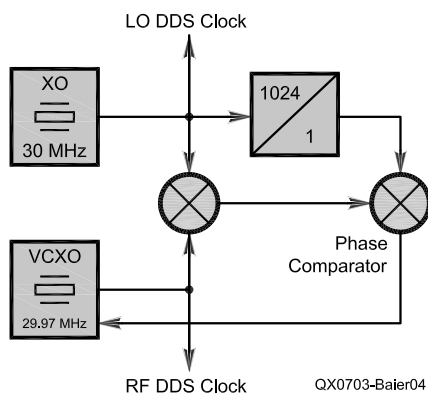


Figure 4 — Generation of two interlocked DDS clocks via phase locked loop.

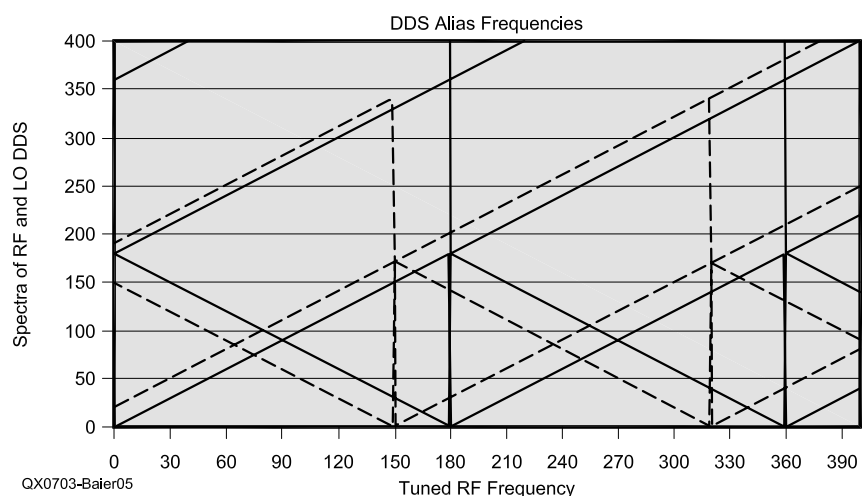


Figure 5 — Utilization of DDS alias frequencies. The RF spectrum is plotted solid; the LO spectrum is plotted dashed. Obviously, there is only one frequency pair mixing to the example IF, which is chosen to 10 MHz for better visibility. In this calculation LO-DDS and RF-DDS clocks are chosen as 170 MHz and 180 MHz, respectively.

3. Measure reference and reflect signals or reference and through signals.
4. Calculate S_{11} or S_{21} .
5. Plot data point to the screen.
6. Repeat measurement cycle with new test frequency at step 1.

Here the timing is the real challenge. Care has to be taken that the measured signals can precisely be related to the set test frequency. On the other hand, the sweep time should be as short as possible (up to 1000 frequency points per second). Finally the software should run under the widespread Microsoft *Windows 2000* or *XP* operating system, which makes coding challenging, since Microsoft *Windows* is not a real-time operating system.

Additionally, the standard PC contains a multitude of clock oscillators that are usually not synchronized with each other. The important clocks for the VNWA application are the

sound card clock oscillator, determining the sampling rate; a performance counter, which can be used to measure points in time with a resolution of about 1 microsecond; and the *Windows* multimedia timer which can fire up to 1000 *Windows* events per second. The latter is used to increment the test frequency. Since the multimedia timer fires quite randomly, even though the average firing rate is quite precise, it is necessary to measure the time of every frequency increment event with the performance counter and memorize it for the further analysis. Now these points in time need to be relocated precisely in the

audio data stream coming from the sound card. Since the sound card clock is usually decoupled from the rest of the PC and on top is not very accurate, it needs to be measured once against the *Windows* performance counter for a later time calibration. Additionally, the time delay between the actual start of the audio acquisition and the sending of the *Windows* command that starts acquisition is unknown. This time delay depends on the actual sound card hardware and on the set sampling rate. It can amount to up to 1 millisecond! I measure it once with a correlational method for time calibration. These two time

calibration data enable us to exactly find the data segment in the audio stream that belongs to a certain test frequency.

Building Blocks

Oscillators

DDS-oscillators⁷ are a perfect choice to generate the RF and LO signals. They offer crystal stability, low phase noise and their frequency can be controlled digitally—and fast—with millihertz resolution. DDS oscillators work similarly to CD audio players. They approximate the wanted sine signal with a step function generated by a D/A converter. Because of this approximation, their output spectrums do not only contain the wanted frequency, but also quite a number of aliased frequencies. Figure 3 shows the unfiltered output spectrum of a DDS oscillator. Usually these aliasing frequencies are unwanted and blocked with a low-pass filter. Since real low-pass filters do not exhibit infinitely steep skirts, DDS oscillators can practically be used to generate sine wave signals of up to about one third of the DDS clock frequency. I selected an AD9851 with a maximum 180 MHz internal clock frequency, which can therefore generate sine waves up to about 60 MHz. I used this DDS type because its package is still big enough to be manually solderable with a soldering iron and I could use an available PC-board layout for my experiments.⁸

However, I soon found that the limited frequency range and the necessity for high-suppression filters (with their temperature stability problems) were bugging me. So I thought about how to explicitly make use of the DDS aliasing frequencies instead of suppressing them. I had to avoid all the aliasing frequencies of the RF oscillator mixing with those from the LO to the very same IF. The simple solution was to use slightly different clock frequencies for the two DDS oscilla-

tors. Experiments revealed that the two clocks must be tied to each other with a PLL circuit. Otherwise strong fluctuations of the IF would occur and deteriorate the phase accuracy. Figure 4 shows how I have generated the two interlocked clock frequencies of 30 MHz and 29.97 MHz with a simple PLL circuit. The 30 MHz XO signal is divided by 1024. The resulting 30 kHz signal is locked to the frequency difference obtained by mixing the XO signal with a 29.97 MHz VCXO signal. Alternatively, another AD9851 could be used to generate the 29.97 MHz clock out of the original 30 MHz DDS clock. This is possible since the AD9851 contains an internal clock multiplier $\times 6$.

Figure 5 shows an example calculation of how any aliasing frequency can be selected for the measurement by appropriate choice of the RF to LO offset. As can be seen from Figure 4, the DDS output power becomes zero at integer multiples of the DDS clock frequency f_{clock} . In the vicinity of these frequencies no measurements are possible because of lack of signal power.

Interference due to the lack of anti-aliasing filters occurs at frequencies where two spectral lines cross, for example at $0.5 \times f_{\text{clock}}$, $1.5 \times f_{\text{clock}}$, $2.5 \times f_{\text{clock}}$ Thus, with some exceptions, the usable frequency range of the VNWA is extended dramatically.

Figure 6 displays the measured convolution

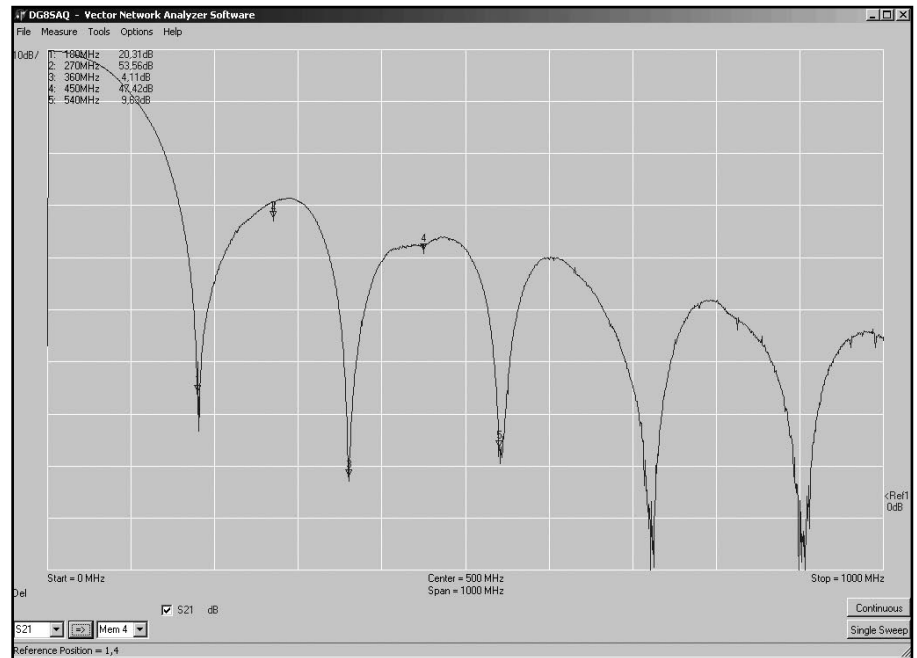


Figure 6 — Reference signal amplitude measured with the VNWA. Clearly, the structure resembles Figure 3.

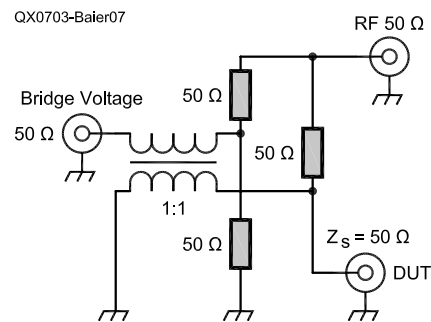


Figure 7 — Standard SWR bridge design.

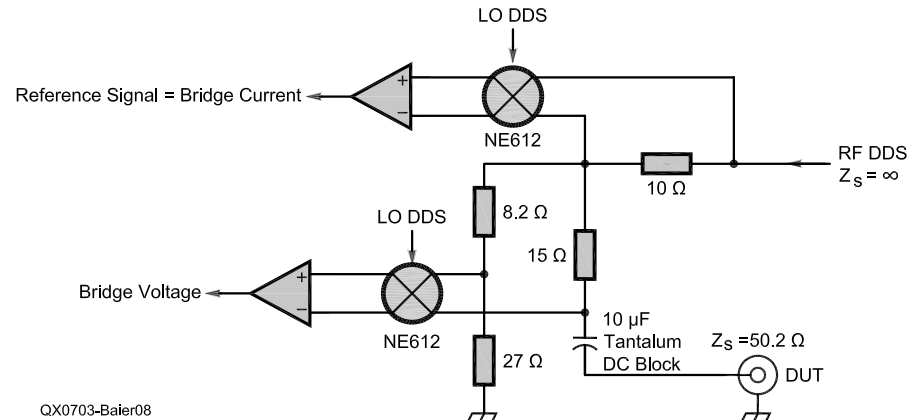


Figure 8 — Modified SWR bridge of the VNWA.

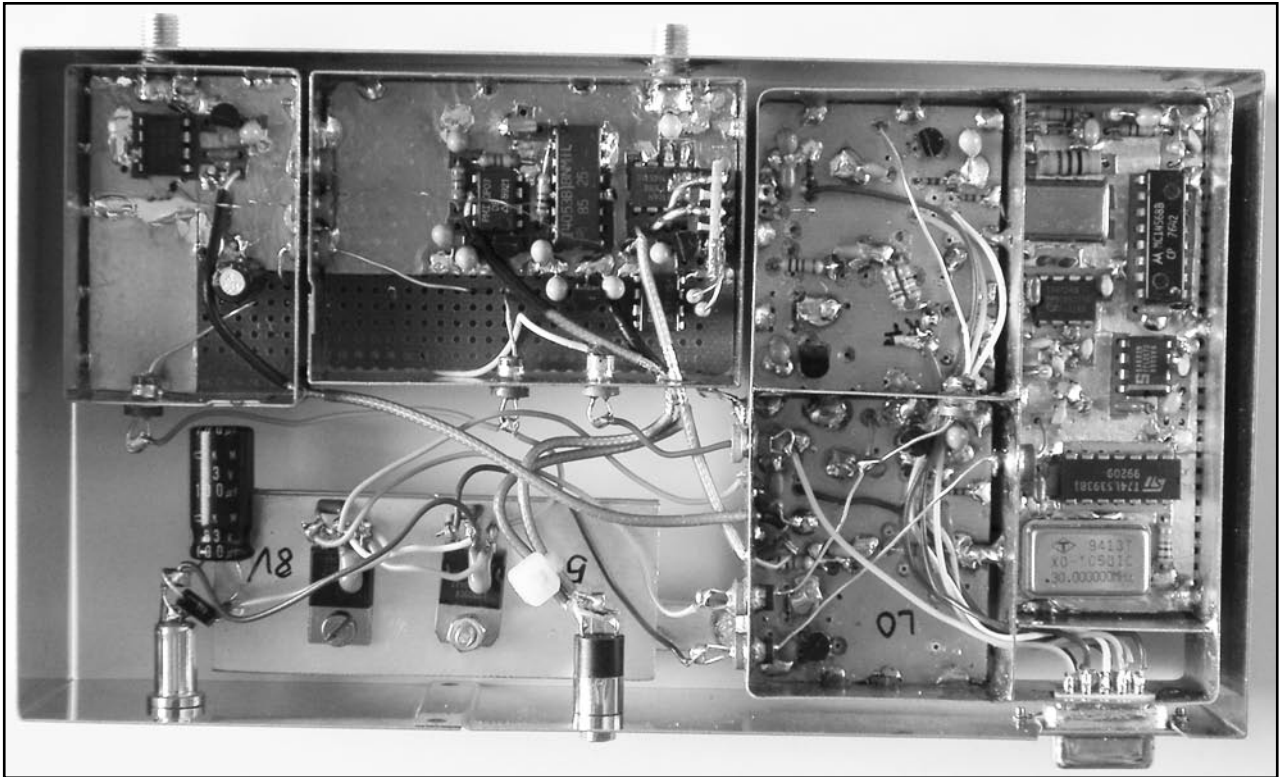


Figure 9 — Top view of the VNWA. From left to right one recognizes: RX mixer, TX mixers, DDS-oscillators, clock generator. Outer dimensions are 185 x 100 x 40 mm.

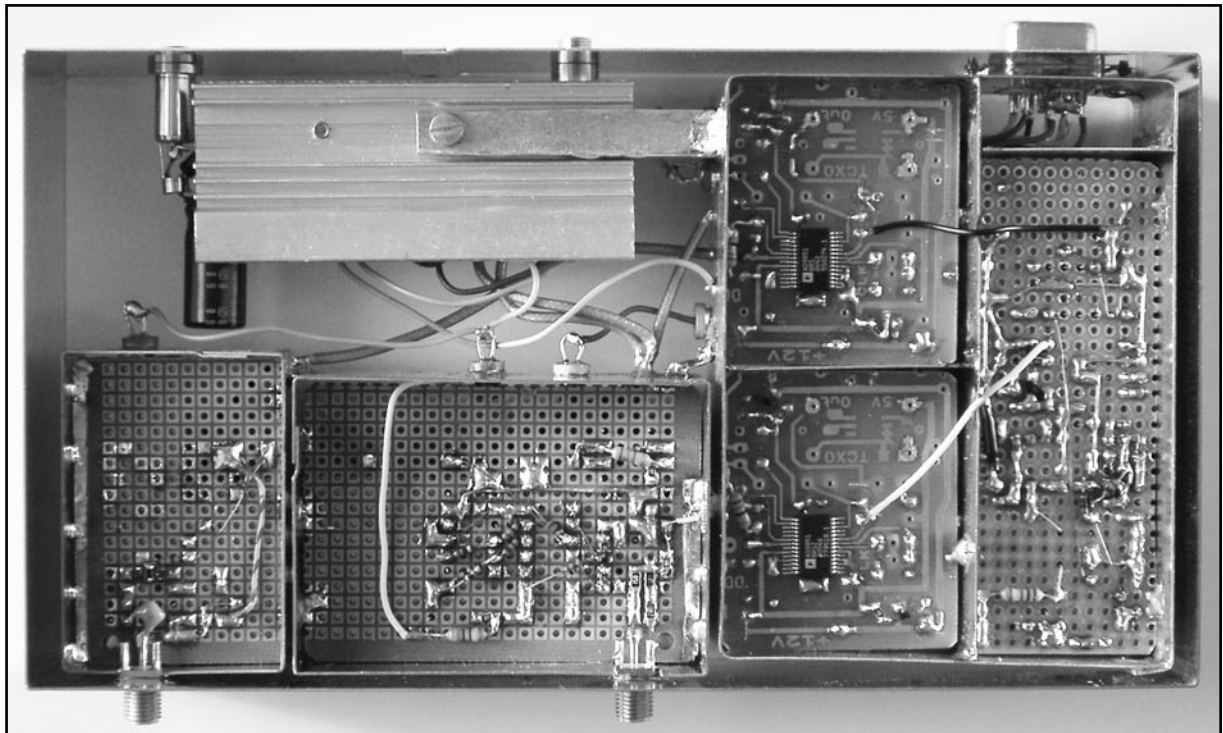


Figure 10 — Bottom view of the VNWA. Here, the two DDS chips and the SWR bridge can be seen.

of the RF and LO DDS spectra in the frequency range 0-1 GHz. It was obtained by detecting the reference signal amplitude with my homebrew VNWA. Clearly the spectral structure of Figure 3 can be recognized. Precise measurements can be performed in the frequency range 200 Hz to 160 MHz and 200 MHz to 330 MHz. Measurements in the 70 centimeter amateur band and above are still possible but are limited in precision because of low signal strength and poor mixer performance. It is remarkable that at 1 GHz a signal can still be detected stronger than 30 dB above the noise level.

SWR Bridge and Mixer

Since I wanted to use my VNWA down to the audio frequency range, I could not use a directional coupler or a hybrid coupler for the reflection measurement, as in the designs of Notes 1 and 2. Instead, I selected a simple Wheatstone type SWR bridge, which works theoretically from dc to several GHz. Figure 7 shows the schematic of such an SWR bridge. This bridge type can readily be found in commercial equipment.⁹ An important feature of SWR bridges is the well-defined 50-Ω source impedance at the DUT port as discussed above. In our example, this is guaranteed when all other ports are terminated with 50 Ω. The bridge voltage is detected through a 1:1 balun. It depends on the input impedance of the DUT and becomes zero if the DUT impedance is 50 Ω. Since it's close to impossible to build a passive BALUN operating from a few hertz to UHF, I used a generic balanced Gilbert-cell mixer of type NE612 instead to detect the bridge voltage. The same mixer type is also used for down conversion of the reference and through signals.

Because of its high input impedance of about 1 kΩ and the fact that the DDS output is a current source with almost infinite source impedance, the bridge resistor values required some redesign. Figure 8 shows my SWR bridge, which works nicely with standard resistor values. My prototype, which is built with non pre-selected resistors, achieves a directivity of 30 dB at 160 MHz. Also important: A good fraction of the DDS output power reaches the DUT.

At this point, I started to consider what signal the SWR bridge exactly measures. I considered the bridge as a 4-port device with the DDS connecting to port 1, port 2 connecting to the reference path, port 3 connecting to the reflect path and port 4 connecting to the DUT. Most interestingly, I found that no matter what the bridge S matrix looks like, the measured signal $M = \text{reflection signal} / \text{reference signal}$ always depends on the reflection coefficient S_{11} of DUT in the very same way:

$$M = \frac{a \cdot S + b}{c \cdot S + 1} \quad [\text{Eq } 2]$$

If the bridge is of perfect design, then the constants b and c are zero (basic function of a good SWR bridge). In reality, the three numbers a, b and c have to be found with the aid of three calibration measurements. These are performed with three different well known terminations, the so-called calibration standards. Usually the standards are chosen to be short, open and load=50 Ω.

Coming back to the hardware, I use a

CMOS switch matrix CD4053 to multiplex the reflected and the through signals. To improve the switch isolation from 50 dB to 100 dB, I use low-resistance HexFETs to short the unselected switch inputs. Finally, the two IF signals are amplified by a factor of 10 with differential amplifiers built out of op amps of type OP07 before they are fed into the sound card. Figures 9 and 10 show my prototype VNWA built into a 185 × 100 ×



Figure 11 — Complete measurement setup with a monolithic crystal filter connected.

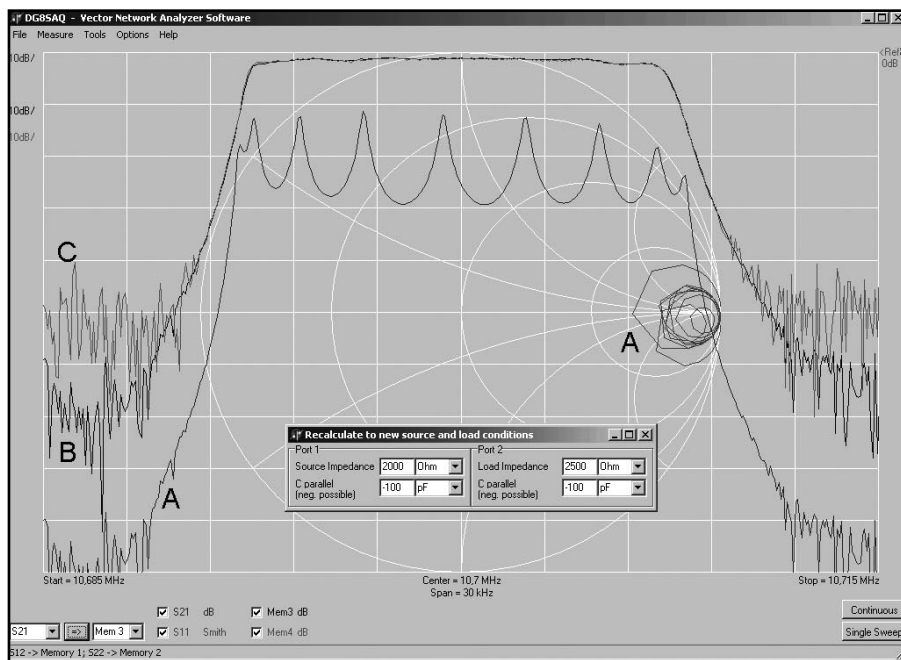


Figure 12 — Unmatched (A) and numerically matched (B) S-parameters of a 10.7 MHz monolithic crystal filter. For comparison, a numerically matched reference measurement obtained on an HP8753C is also plotted (C). The color version is available at www.arri.org/qexfiles/3x07_Baier.zip.

40 mm sheet-metal enclosure. Except the DDS part, all components have been assembled onto experimental multipurpose PC boards that have been covered on the upper side with thin adhesive copper sheets for grounding and shielding. Figure 11 shows the complete measurement setup with a monolithic crystal filter connected to the VNWA.

Test Results

Figure 12 shows S parameters of a 10.7 MHz monolithic crystal filter measured with 50 Ω source and load impedance (A). Because of the strong impedance mismatch between filter and VNWA, the filter transmission shows a considerable passband ripple. With a simulation tool embedded in my VNWA software, I have recalculated the measured filter S parameters to a 2000 Ω / 2500 Ω impedance environment (B). In addition, a reference measurement obtained on a HP8753C is also recalculated to the high-impedance environment and plotted (C). The match between my VNWA data and the HP8753C data is excellent. Another indicator for the good quality and consistency of the S-parameters measured on my VNWA is that the filter passband becomes perfectly smooth after impedance transformation. Erroneous measurements can be recognized by severe spikes in the pass band of high Q devices after impedance transformation as extreme impedance transformations magnify the effect of measurement errors.

Figure 13 shows the measured input reflection coefficients (S_{11}) of two crystals unsoldered from a bridge type crystal filter. I have imported the very same measured S parameters into the simulation tool APLAC in order to calculate how the crystals would behave in a bridge type filter (Figure 14). The simulation results are shown in Figure 15. Apparently the measured S-parameters are well suited for a system simulation.

To test my VNWA at very low frequencies, I measured an old commercial three-pole 11 kHz LC band-pass filter. Figure 16 displays the results. Curve A shows the measured filter transmission in the original 50-Ω impedance environment. The same measurement recalculated to 610 Ω source and load impedances is also plotted (B). Curve C (noisy curve) was obtained by measuring the very same filter with 560 Ω series resistors between VNWA TX port and filter input and between filter output and RX port respectively. The 560 Ω resistors connected in series to the 50 Ω VNWA impedances form 610 Ω source and load impedances for the filter. Obviously, the calculated trace (B) and the measured trace (C) match nicely. Also, an additional insertion attenuation of calculated 21.7 dB caused by the resistors is basically observed. These measurements had been performed with a

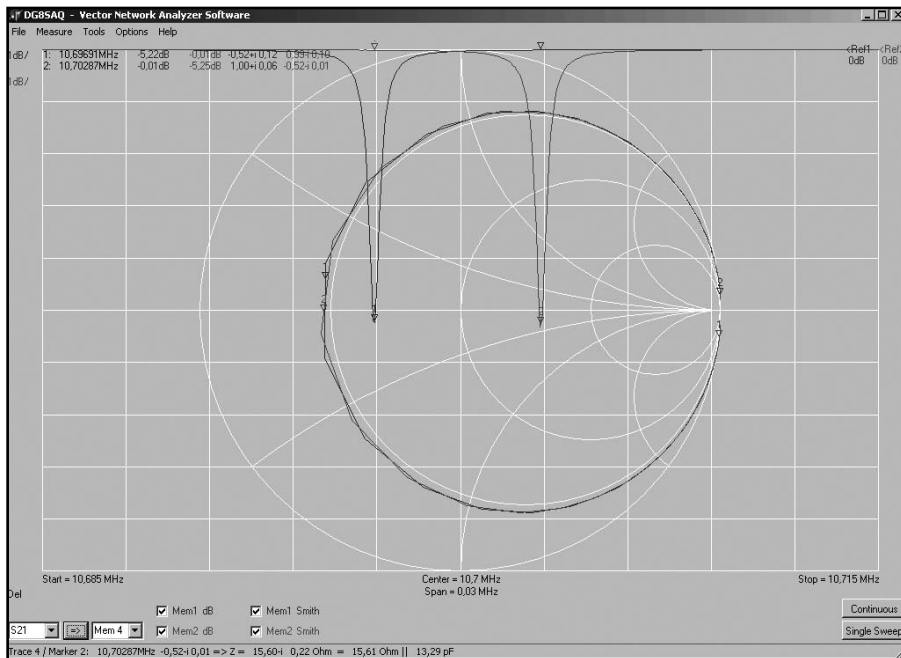


Figure 13 — Reflection coefficients of two different 10.7 MHz filter crystals.

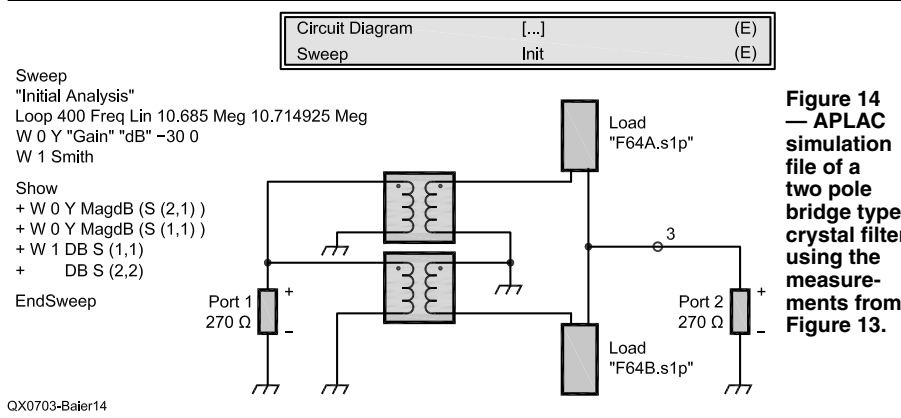


Figure 14 — APLAC simulation file of a two pole bridge type crystal filter using the measurements from Figure 13.

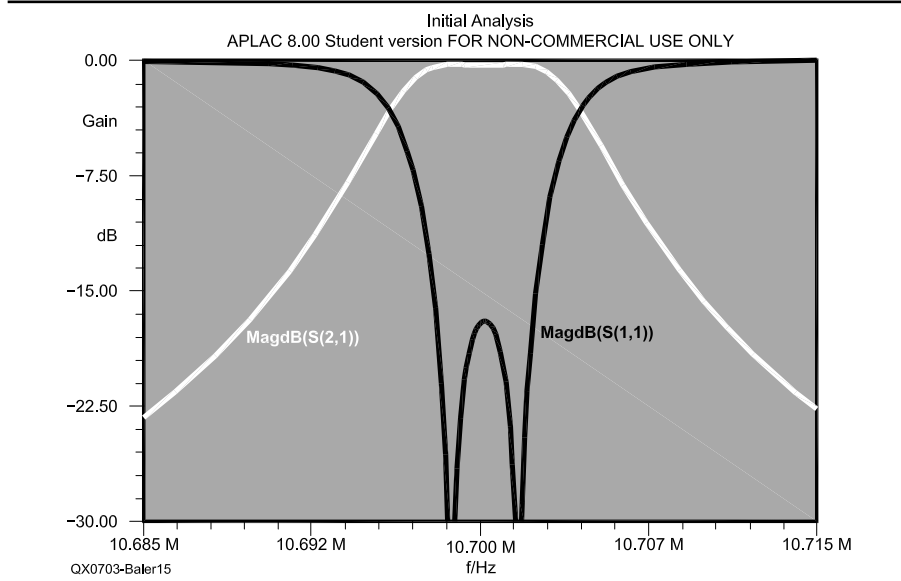


Figure 15 — Simulation results of the bridge type crystal filter from Figure 14.

10 dB coaxial attenuator connected to the VNWA TX port in order to obtain a well-defined 50 Ω source impedance of the TX port. At these very low frequencies, the dc blocking capacitor changes the bridge impedance.

Figure 17 shows a measurement performed in the UHF range. I have measured the S parameters of a 400 MHz crystal surface acoustic wave IF filter out of a GSM mobile phone (A). The reference measurements obtained on a HP8753C (B) prove that measurements are still possible at this high frequency range. The dynamic range is limited but impedances can still be measured reasonably accurately for Amateur Radio purposes. Figure 18 displays the very same measurements recalculated to 550 Ω source and load impedances, with inductors equivalent to negative capacitors of -40 pF connected in parallel to the filter input and output. Apparently, the obtained S parameters are still good enough to calculate a matching network. A 10 dB coaxial attenuator in front of the RX port additionally degraded the dynamic range during this measurement. It was necessary to obtain a well defined 50 Ω load impedance at the filter output.

Summary and Outlook

I have described a very simple homebrew PC supported vector network analyzer which operates on all Amateur Radio bands below 500 MHz and even beyond. The wide operating frequency range was obtained by deliberately using aliasing frequencies generated by the DDS oscillators. The simplicity of design was reached by utilizing an IBM compatible PC to the greatest extent possible. The parallel printer port was used for control and the sound card was used for data acquisition. With this setup, a measurement resolution of 0.01 dB and 0.1° can be achieved. A dynamic range of over 100 dB can be reached.

The concept offers many possibilities for further improvement. With higher clocked DDS chips (for example, AD9858, 1 GHz clock) and improved mixers, the frequency range could simply be extended to beyond 2 GHz. Look at Note 10 for new developments and for my most recent VNWA software.

Acknowledgments

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Wolfgang Schneider, DJ8ES for helping me get started with DDS technology.

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Thanks to Stefan Fuchs for support with the reference measurements.

Last but not least thanks to Mike

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Notes

¹Tom McDermott, N5EG, and Karl Ireland, "A Low-Cost 100 MHz Vector Network Analyzer with USB Interface", *QEX*, Jul/Aug 2004,

ARRL. See also www.tapr.org/kits_vna.html.

²Homebrew-VNA by Paul Kiciak, N2PK; n2pk.com/index.html.

³www.aplac.com/.

⁴eesof.tm.agilent.com/products/ads_main.html.

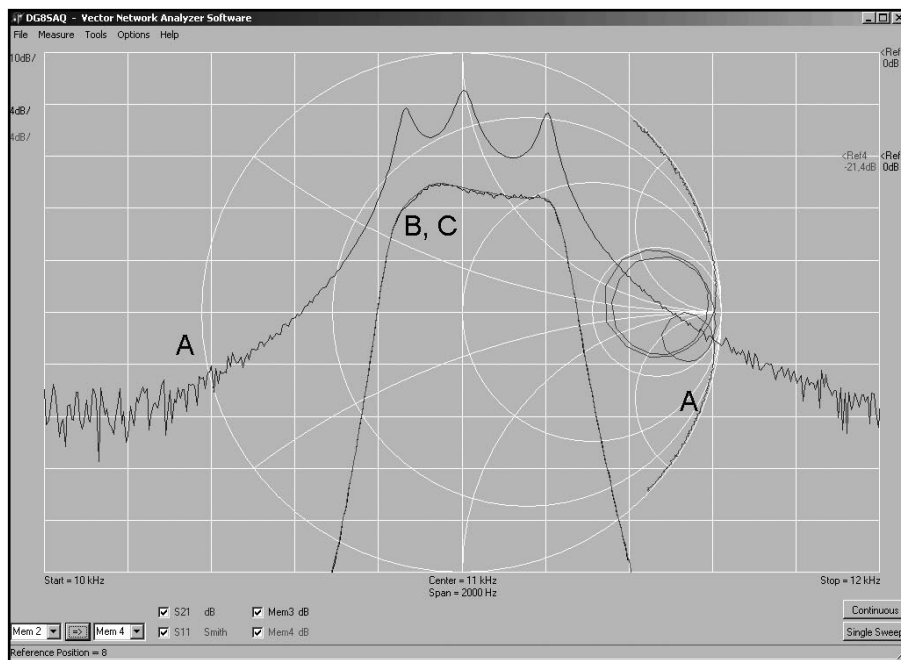


Figure 16 — Unmatched (A, 10 dB/div) and numerically matched (B, 4 dB/div) S-parameters of a three pole 11 kHz LC-filter. A measurement of the same filter matched with two 560 Ω series resistors is also plotted (C, noisy trace, 4 dB/div, 21.4 dB offset to trace B). The color version is available at www.arrl.org/qexfiles/3x07_Baier.zip.

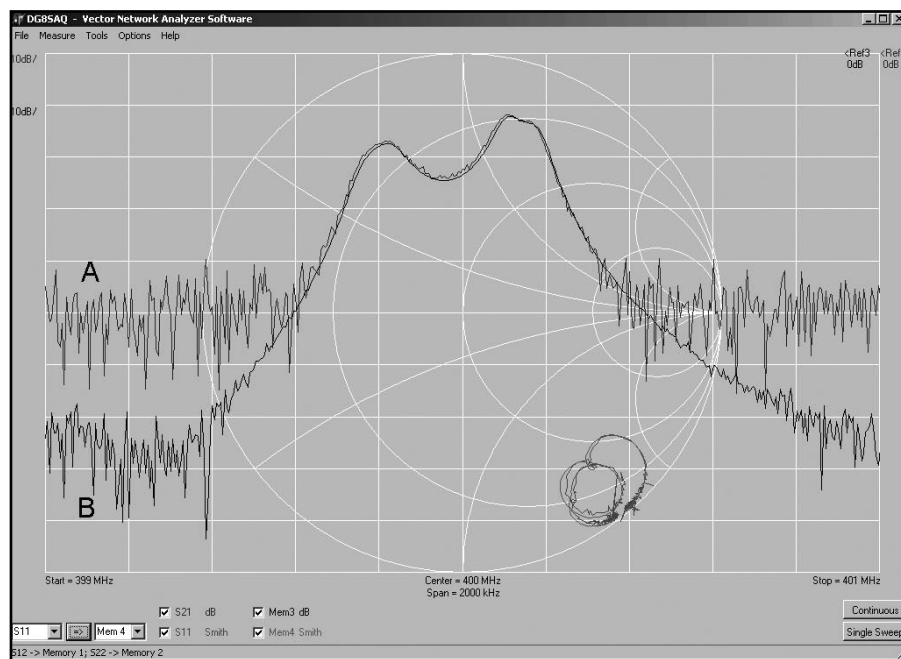


Figure 17 — S-parameters of a 400 MHz crystal surface acoustic wave filter measured with VNWA (A) compared to HP8753C reference measurement (B). The color version is available at www.arrl.org/qexfiles/3x07_Baier.zip.

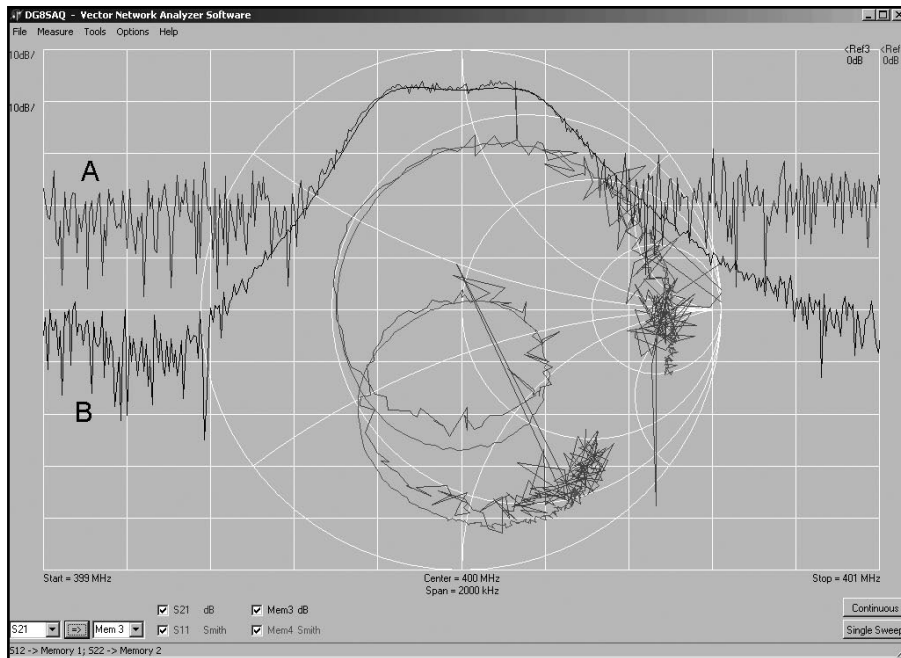


Figure 18 — S-parameters of Figure 17 numerically recalculated to an impedance level of 550 Ω with parallel inductors equivalent to -40 pF.

⁵Sound Blaster Live! 24-bit; www.soundblaster.com.


⁶www.mydarc.de/DG8SAQ/SoundBlaster/index.shtml.


⁷AD9851 data sheet by Analog Devices to be found at www.analog.com. Thanks for the free samples!

⁸C. W. Preuss, WB2V, "Building a Direct Digital Synthesis VFO," *QEX*, Jul 1997, ARRL.

⁹eg, Rohde & Schwarz SWR bridge ZRC.





¹⁰www.mydarc.de/DG8SAQ/VNWA/index.shtml.

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